



## CE-ATA Design Guide

|                     |            |
|---------------------|------------|
| Design Guide ID     | 002        |
| Affected Spec Ver.  | CE-ATA 1.1 |
| Corrected Spec Ver. |            |

### Submission info

| Name       | Company | Date      |
|------------|---------|-----------|
| Echa Chang | Intel   | 1/28/2006 |
| Sumit Puri | Fujitsu |           |

### Description of design guidance

The specification and host supplement is ambiguous regarding the minimum set of MMC commands a CE-ATA host and device is recommended to support in order to achieve MMC layer initialization and bus width switching. The only required commands listed in the specification are CMD0, CMD12, CMD39, CMD60, and CMD61.

This design guide clarifies the MMC commands and MMC registers a CE-ATA device needs to support for MMC initialization and bus width switching.

Detection and initialization of the base MMC device should proceed as defined in the MMC reference. Table 1 lists the minimum set of additional MMC commands the device is recommended to support in order to achieve MMC layer initialization and bus width switching. Note that CMD14 and CMD19 are not listed for bus width discovery. CE-ATA is for embedded systems where it is expected that the bus width to be used is known.

| <b>MMC Layer Initialization</b> |
|---------------------------------|
| CMD1                            |
| CMD2                            |
| CMD3                            |
| CMD7                            |
| <b>MMC Bus Width Switching</b>  |
| CMD8                            |
| CMD6                            |
| CMD13                           |

**Table 1 List of recommended MMC commands**

After MMC layer initialization and bus width switching are complete, it is recommended that the host no longer use commands listed in Table 1. After this point, it is recommended that the host only use CE-ATA commands (CMD0, CMD12, CMD39, CMD60, CMD61). For commands whose response timing requirements are specified by  $N_{AC}$ , for CE-ATA devices the  $N_{ACIO}$  timing parameter should be used instead.

Table 2 lists the set of MMC registers the device is recommended to support in order to achieve MMC layer initialization and bus width switching.

| <b>MMC Registers</b> |
|----------------------|
| OCR                  |
| CID                  |
| RCA                  |
| EXT_CSD              |

**Table 2 List of recommended MMC registers**

The R1 response format contains a 32-bit field named CARD STATUS. It is recommended that the device support this field for proper initialization.

| <b>Status Field</b> |
|---------------------|
| CARD STATUS         |

**Table 3 CARD STATUS field**

#### Disposition log

|           |                                                               |
|-----------|---------------------------------------------------------------|
| 11/1/2006 | Design guide captured.                                        |
| 1/28/2007 | Card Status added and additional input.                       |
| 2/4/2007  | Changes based on 1/31 Digital meeting.                        |
| 2/16/2007 | Changes to reflect bus width initialization.                  |
| 2/26/2007 | Added timing information for CMD8.                            |
| 3/5/2007  | Adjustments to make timing information for CMD8 more general. |
| 4/30/2007 | Erratum ratified.                                             |

*Technical input submitted to the CE-ATA Workgroup is subject to the terms of the CE-ATA contributor's agreement.*